Amendments to the Specification:

Please replace the paragraph beginning on Page 1, line 9, with the following amended paragraph:

The invention relates to a data processor comprising one or more functional units, one or more register files, a data memory, and moreover a snapshot buffer that accommodates to store state ~~informations~~information of the processor during an interrupt condition in respective buffer elements ~~as has furthermore been recited in the preamble of Claim 1~~. For being able to obtain high-quality operation schedules in VLIW and other state of the art processors, ideally all hardware characteristics that are relevant to the compiler should be visible to the compiler. Although not being limited thereto, a particular relevant category of such ~~informations~~information pertains to the various latencies of respectively associated operations. High performance pipelined processors use latency values that are in excess of one, to thereby raise performance. In operation, the latency values should be exactly specified. This implies that not only the total duration of the operation will be specified, but also the precise instants should be known at which specific operations will occupy specific hardware for the consuming of operands, the processing of data, and the production of results. Thereby, superior schedules with minimum register pressure can be obtained.

Please delete the paragraph beginning on Page 3, line 15.

Please replace the paragraph beginning on Page 3, line 17, with the following amended paragraph:

The invention also relates to a data processing facility with such data processor embedded, and to a method for operating a data processor arranged for handling nested interrupts in the above indicated manner. ~~Further advantageous aspects of the invention are recited in dependent Claims.~~

Please replace the paragraph beginning on Page 4, line 23, with the following amended paragraph:

Both the demultiplexor 54 and the multiplexor 56 are controlled by a stack pointer from a stack pointer register 58 that is located in the snapshot buffer as well. In fact, reading from the snapshot buffer on line 62 is only required at the start of a nested interrupt, and writing to the snapshot buffer from line 60 is only required at the end of a nested interrupt. Therefore, these two operations will never occur simultaneously and a single pointer register 58 could be sufficient to control the interleaved addressing of different words in the stack buffer. The pointer value is retrocoupled on line ~~62~~ 64 to pointer update control 66 for subsequent reloading of pointer register 58. As shown, three-operation control line 68 will allow respective read, write, and no-operation modes with respect to the pointer value. The effective operations are executed in decrementing element (-1), incrementing element (+1), and no-operation element (through a straightaway retrocoupling).